300 GHz Path Loss Measurements on a Computer Motherboard

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Abstract—This paper presents the 300 GHz path loss measurements on a computer motherboard. In the measurement campaign, three different scenarios have been considered: a line-of-sight (LoS) scenario in the presence of a large ground plane (i.e., motherboard), a LoS scenario where the transmitter (Tx) and receiver (Rx) have different heights such as a link between the processor and memory, and an obstructed LoS scenario where the EM waves are guided from the Tx to the Rx through the metal parallel-plate structures such as Dual In-line Memory Modules (DIMM’s) on the motherboard. The results show that in the presence of the motherboard, LoS path can be positively or negatively interfered by the reflections from the ground plane. The outcome strongly depends on the antenna position with respect to the motherboard. Furthermore, it is found that if the Tx and Rx antennas are not on the same height, the height difference of less than a centimeter between antennas is tolerable. However, the height difference of several centimeters, as found in links between the processor and memory, would suffer from significant path loss. Finally, it was found that the chip-to-chip link that is obstructed by a parallel metal plates can experience both path loss higher or lower than free space path loss, depending on the spacing between metal plates. All these results indicate that optimal communications can be achieved by carefully positioning the antennas with respect to the motherboard layout.

I. INTRODUCTION

Data communication between computer components, such as processor and memory within a computer system, currently relies on metal wires and a transition to optical waveguides is expected in the future. While optics promise much higher data rates, the usable frequency band around each frequency is much larger, so each channel can have a much higher data rate. This alone can increase data rates to several tens of Gbits/s, but multiplexing (MIMO) is still needed to reach Tb/s data rates. Fortunately, THz frequencies allow smaller antennas and antenna spacing, which provides for more MIMO channels within the same array aperture within a chip package. Finally, THz wireless offers some potential advantages relative to free-space optical communication because THz wireless also allows wireless communication within a system where free-space optical faces the problem of getting out of and into the chip package.

To enable chip-to-chip THz wireless communications, it is imperative to understand propagation mechanisms that govern communication in the unique propagation environment of a computer system (motherboard) at these high frequencies. While measurements on the computer motherboard have been reported at lower frequencies [18]-[20], to the best of our knowledge, no channel measurements in the computer motherboard environment at 300 GHz have been reported in the open literature. As the first step toward characterizing 300 GHz chip-to-chip channel on a motherboard, we have performed path loss measurements in Line-of-Sight (LoS) and Obstructed-Line-of-Sight (OLoS) environments at 300 GHz with 20 GHz of bandwidth. In this measurement campaign, three different scenarios have been considered: a LoS scenario in the presence of a large ground plane (i.e., motherboard), a LoS scenario where the transmitter (Tx) and receiver (Rx) have different heights such as a link between the processor and memory, and an OLoS scenario where the EM waves are guided from the Tx to the Rx through the metal parallel-plate structures such as Dual In-line Memory Modules (DIMM’s) on the motherboard. The results show that in the presence of the motherboard, LoS path can be positively or negatively obstructed by the reflections from the ground plane. The outcome strongly depends on the antenna distance from the motherboard. For example, just a few millimeters of variation
in the antenna height results in an increase or decrease in path loss by as much as 3 dB, depending on the nature of interference (i.e., destructive or constructive) between the LoS path and the ground-reflected path. Furthermore, it is found that if the $T_x$ and $R_x$ antennas are not on the same height, the height difference of less than a centimeter between the antennas is tolerable. However, the height difference of several centimeters, as found in links between the processor and memory would suffer from significant path loss. Finally, it was found that the chip-to-chip link that is obstructed by a parallel metal plates can experience both path loss lower or higher than the free space path loss, depending on the spacing between metal plates. All these results indicate that optimal communications can be achieved by carefully positioning the antennas with respect to motherboard layout.

The remainder of this paper is organized as follows: Section II briefly describes the measurement equipment and the antennas used in the measurements. Section III describes measurement scenarios, while Section IV discusses the path loss measurement results. Finally, Section V provides some concluding remarks.

II. Measurement Setup

The measurement setup consists of the N5224A PNA vector network analyzer (VNA), the VDI transmitter (Tx210) and the VDI receiver (Rx148). The N5224A PNA VNA provides input signal in the range 10 MHz-20 GHz. In the VDI Tx210 transmitter, the THz-range carrier signal starts out as a 25 GHz signal, which is generated by a Herley-CTI phase-locked dielectric resonator oscillator (DPRO with 100 MHz reference crystal oscillator) [21]. This signal is amplified and its frequency is doubled using Norden N08-1975 [22], and then its frequency is tripled using VDI WR6.5X3 [23]. This signal is then fed to a sub-harmonic mixer (WR2.8SHM) that plays a dual role of doubling the carrier frequency and mixing it with the baseband signal (10 MHz–20 GHz, delivered by the VNA) [24]. The terahertz-range signal is then transmitted by the high-gain horn antenna in the range 280-320 GHz. At the receiver side, the same components are used to down-convert the signal, except that the DPRO is tuned to 24.2 GHz. This results in a down-conversion of the received signal to an intermediate frequency (IF) of 9.6 GHz. The upper sideband of the down-converted signal is then recorded by the VNA in the frequency range of 9.6-29.6 GHz. The antenna used in the measurement is a pyramidal horn with gain that varies from 22 to 23 dBi from 300 GHz to 320 GHz, respectively. Both $T_x$ and $R_x$ antennas are vertically polarized and mounted about 1.5 cm above the ground. The theoretical half power beam-widths (HPBW) are about 10° in azimuth and elevation. More details on the measurement setup can be found in [25].

III. Measurement Scenarios

In this measurement campaign, three different scenarios have been considered: LoS propagation between the $T_x$ and $R_x$ over the large ground plane (i.e. motherboard) as shown in Fig. 1, a LoS scenario where the $T_x$ and $R_x$ have different heights like in processor-memory link (denoted as A-B link) shown in Fig. 2, and an OLoS scenario where the EM waves are guided from the $T_x$ to the $R_x$ through the metal parallel-plate structures such as DIMM’s on the motherboard (denoted as C-D link) shown in Fig. 2.

![Fig. 1. LoS propagation between the Tx and Rx over the motherboard.](image1)

![Fig. 2. LoS processor-memory link (A-B) and OLoS link (C-D) through guided wave structure.](image2)
B. Processor-Memory Link (A-B Channel)

One of the main application for THz wireless chip-to-chip communications on a motherboard is a processor to memory link. Hence, we have measured a path loss of a processor-memory link denoted as A-B channel in Fig. 2. From the figure, we can observe that it is difficult to have a clear LoS link in an environment that has such high density of components. Furthermore, the positions of the chips on the motherboard are not coplanar, but rather 3-D, since the memory cards are inserted vertically in the slots and the processor is near the surface of a motherboard. To study the impact of different antenna heights when directional antennas are used, we have set up the T_x and R_x antennas in A and B points, respectively. The difference in T_x and R_x antenna heights was 4.3 cm, and the T_x-R_x separation distance, d has been increased by moving the R_x module in 2 cm increment from 16.2 cm to 26.2 cm.

C. OLoS Link through Guided Metal Parallel-plate Structures (C-D Channel)

Another important scenario for chip-to-chip communications is when the LoS link is perturbed by a parallel metal-plate structures such as C-D link in Fig. 2. Here, we have investigated whether these metal walls can act as parallel-plate waveguides or just introduce multipath propagation. The structural resemblance can also be found with the vertically inserted DIMM’s. On the motherboard, due to its compact, highly dense configuration, it is difficult to differentiate the impact that one component has on the wave propagation from that of the other. For example, the effects of cylindrical capacitors present between the two DIMM’s that would scatter or diffract the waves need to be differentiated from the wave-guiding effect of the DIMM’s. Therefore, as shown in Fig. 3, we isolate the local propagation environment of this particular chip-to-chip scenario and re-construct it on the backside of the motherboard. The figure also shows the corridor width, w, which has been varied from 1.7 cm to 5.2 cm to see how path loss changes with increasing or decreasing width.

Fig. 3. Measurement setup for DIMM as a waveguide.

IV. MEASUREMENT RESULTS

The measurement results for the three measurement scenarios described in Section III are presented and analyzed in this section. Here, we refer to measured path loss, PL, as the transmit power, P_t, multiplied by the transmit and receive antenna gains, G_t and G_r, respectively, divided by the received power, P_r, i.e.,

$$PL = \frac{P_t \cdot G_t \cdot G_r}{P_r}.$$  (1)

The measured path loss is compared with the theoretical Friis formula defined as [26]

$$\bar{PL} = \left(\frac{4\pi d}{\lambda}\right)^2,$$  (2)

where d is the T-R separation distance, and λ is the wavelength.

The mean path loss, $\overline{PL}$, is obtained by averaging a swept continuous wave over time and frequency, i.e.,

$$\overline{PL}(d) = \frac{1}{MN} \sum_{i=1}^{N} \sum_{j=1}^{M} |H(f_i,t_j,d)|^2,$$  (3)

where $H(f_i,t_j,d)$ is the measured complex frequency response data matrix, N is the number of observed frequencies, M is the number of frequency-response snapshots over time, and d is the distance in meters.

A. Path Loss of LoS over a Large Ground Plane

Figure 4 compares the measured and theoretically calculated path loss curves for the experimental setup described in Section III-A. First, we can observe that all measured path loss curves have oscillations. These oscillations are the result of the strong reflections that arrive at the receiver after multiple reflections of the back of the T_x/R_x electronics, as it has been reported [25]. Furthermore, we can observe that the measured path loss when both the T_x and R_x are h = 2.1 cm above the ground plane follows well Friis formula prediction. This is not a surprising result due to narrow bemawidths of the antennas and confirms that the ground reflected path does not exist at these antenna heights. For antennas positioned on the motherboard, the ground reflection destructively interferes with the LoS, resulting in about 3 dB higher path loss than what is predicted by Friis formula. On the other hand, when the horns are 8 mm above the board (h = 0.8 cm), the two paths constructively interfere, and the measured path loss actually becomes slightly lower than the theoretical curve. Another interesting observation from Fig. 4 is that for the same height of 0 cm, path loss is reduced by 3 dB when the antennas are placed over a section of the board that has higher solder pin density (referred to as h = 0 cm solder pin in Fig. 4). This is because the amplitude and phase of the ground reflected signal is changed due to the higher reflectivity and surface roughness of the solder-pin-populated surface, such that the amplitude of the resultant vector sum at the receiver is slightly increased.
B. Path Loss of Processor-Memory A-B Link

Link A-B shown in Fig. 2 describes a typical processor to memory link where the $T_x$ and $R_x$ antennas are not on the same height. Figures 5 and 6 illustrate how the measured path loss varies with the change in the distance between the $T_x$ and $R_x$, and with the antenna height, respectively.

Fig. 5 shows the measured path loss for different T-R separation distances with 4.3 cm of height difference between $T_x$ and $R_x$, and compares them with corresponding theoretical values obtained from Friis formula. We can observe that the path loss is higher for shorter distances compared to longer distances. While this may seem counterintuitive, because of the geometrical structure is very possible. Note that the antennas have high directivity and narrow beamwidth and that height difference of 4.3 cm creates very obstructed LoS propagation.

On the other hand, as the distance increases, the $T_x/R_x$ antennas start falling within each others’ beamwidths, and more of the LoS power as well as the ground-reflected power is detected toward the receiver. This results in less path loss as the distance increases. However, note that even at maximum distance of 26.2 cm, the height difference of 4.3 cm introduces loss of about 15 dB with significant fluctuation in path loss. This result indicates that the A-B link is probably not a reliable channel, which raises the following question: how much height difference between $T_x$ and $R_x$ antennas are tolerated?

Fig. 6 shows measured path loss for different heights of the $R_x$ antenna when the $T_x$ antenna is fixed at the height 2.1 cm from the motherboard ($h_{T_x} = 2.1$ cm). It is observed from the figure that for the height difference between the $T_x$ and $R_x$ less than 1.3 cm, the measured path loss matches the theoretical value, while for greater height difference, measurements start to deviate from the Friis line with greater fluctuation in the path loss. From these results, we can conclude that the LoS chip-to-chip wireless channel on the horizontal plane (on motherboard surface) with minor $T_x/R_x$ height difference is feasible, while the link between two chips, whose height difference is in the order of few centimeters, such as channel A-B, will suffer from significant loss.

C. Path Loss of OLoS C-D Link

Another important scenario for chip-to-chip communications is when the LoS link is perturbed by a parallel metal-plate structures such as C-D link in Fig. 2. Fig. 7 shows the measured path loss results for different distances between the two DIMM’s. First, we can observe that the path loss increases significantly above the theoretical level for $w = 2.3$ cm indicating that multipath reflections are superimposed in destructive manner. On the other hand, for $w = 3.3$ cm, the path loss is lower than predicted by Friis formula, indicating that the multipath reflections are superimposed in constructive manner. Finally, for $w = 5.2$ cm, the measured path loss returns to the theoretical level. What can be inferred from this result is that there exist multipath components inside the corridor created by the two DIMM’s: LoS and a path bouncing between the memory plates. The amplitude, phase,
and delay of the bounced path is determined by the width of the corridor, $w$. These results indicate that this channel can be used for chip-to-chip communications with careful selection of spacing between memory plates. Here, we also note that the oscillations in the measured path loss curves are still visible since the reflections between the $T_x$ and $R_x$ back panels exist in the LoS channel. In this measurement setup, we made sure that the $T_x/R_x$ antenna heights are set to 2.1 cm from the motherboard to ensure that the measured path loss is not affected by the ground reflection, as it has been found in Section III-A.

![Fig. 7. Measured path loss curves for different distances between the two DIMM’s.](image)

V. CONCLUSIONS

This paper presents the 300 GHz path loss measurements on a computer motherboard. In the measurement campaign, three different scenarios have been considered: a line-of-sight (LoS) scenario in the presence of a large ground plane (i.e. motherboard), a LoS scenario where the transmitter ($T_x$) and receiver ($R_x$) have different heights such as a link between the processor and memory, and an obstructed LoS scenario where the EM waves are guided from the $T_x$ to the $R_x$ through the metal parallel-plate structures such as DIMM’s on the motherboard. The results show that in the presence of the motherboard, LoS path can be positively or negatively affected by the reflections from the ground plane. The outcome strongly depends on the antenna position with respect to the motherboard. Furthermore, it is found that if the $T_x$ and $R_x$ antennas are not on the same height, the height difference of less than a centimeter between antennas is tolerable. However, the height difference of several centimeters, as found in links between the processor and memory would suffer from significant path loss. Finally, it was found that the chip-to-chip link that is obstructed by a parallel metal plates can experience both path loss higher or lower than free space path loss, depending on the spacing between metal plates. All these results indicate that optimal communications can be achieved by carefully positioning the antennas with respect to the motherboard layout.

REFERENCES


